AC'97 SoundMAX® Codec

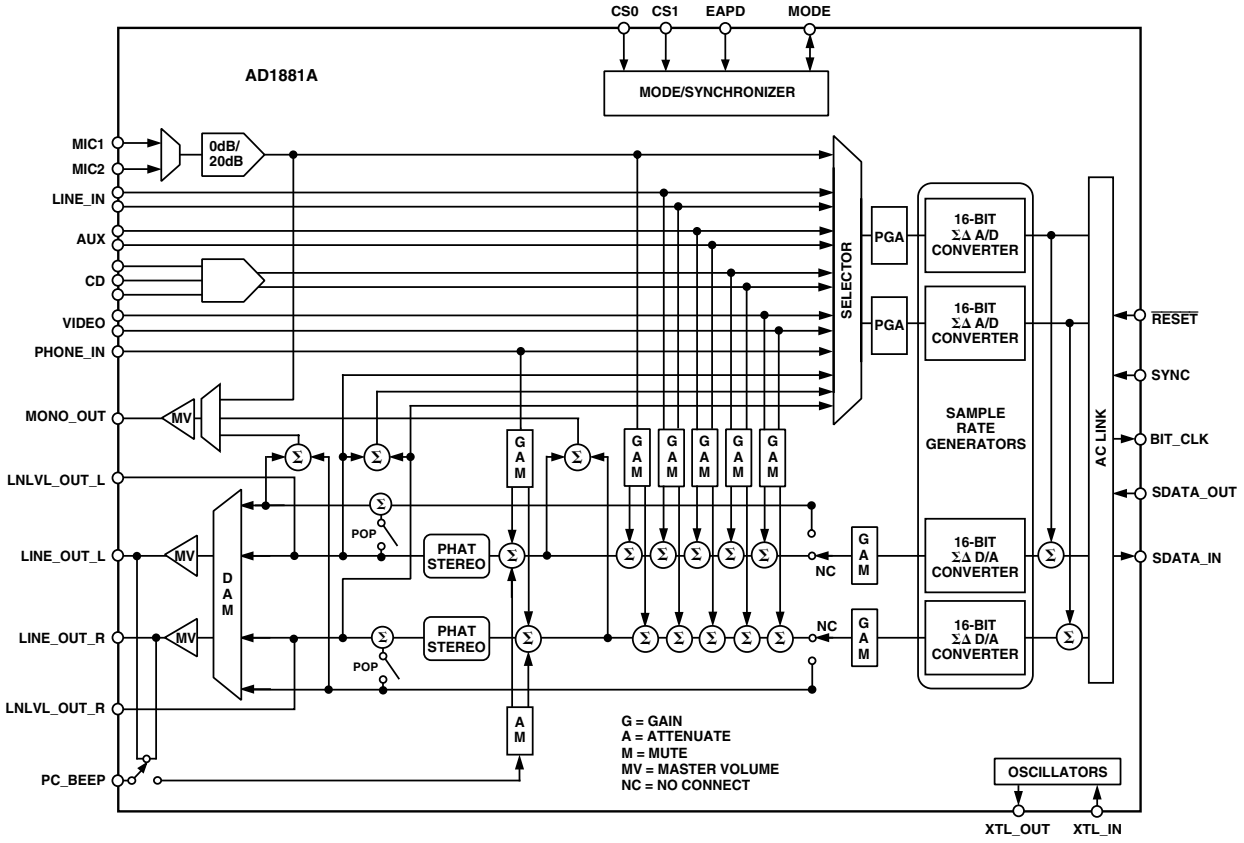
AD1881A

AC'97 2.1 FEATURES
Variable Sample Rate
True Line-Level Output
Supports Secondary Codec Modes

AC'97 FEATURES
Designed for AC'97 Analog I/O Component
48-Lead LQFP Package
Multibit ΣΔ Converter Architecture for Improved S/N Ratio Greater than 90 dB
16-Bit Stereo Full-Duplex Codec
Four Analog Line-Level Stereo Inputs for Connection from LINE, CD, VIDEO, and AUX
Two Analog Line-Level Mono Inputs for Speakerphone and PC BEEP
Mono MIC Input Switchable from Two External Sources
High Quality CD Input with Ground Sense
Stereo Line-Level Output
Mono Output for Speakerphone or Internal Speaker
Power Management Support

ENHANCED FEATURES
Mobile Low Power Mixer Mode
Digital Audio Mixer Mode
Full Duplex Variable 8 kHz to 48 kHz Sampling Rate with 1 Hz Resolution
PHAT™ Stereo 3D Stereo Enhancement
Split Power Supplies (3.3 V Digital/5 V Analog)
Extended 6-Bit Master Volume Control
Audio Amp Power-Down Signal

FUNCTIONAL BLOCK DIAGRAM



SoundMAX is a registered trademark and PHAT is a trademark of Analog Device, Inc.

REV. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
© Analog Devices, Inc., 2000

AD1881A–SPECIFICATIONS

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25	°C
Digital Supply (V_{DD})	3.3	V
Analog Supply (V_{CC})	5.0	V
Sample Rate (F_S)	48	kHz
Input Signal	1008	Hz

DAC Test Conditions
Calibrated
–3 dB Attenuation Relative to Full-Scale
Input 0 dB
10 kΩ Output Load

ADC Test Conditions
Calibrated
0 dB Gain
Input –3.0 dB Relative to Full-Scale

ANALOG INPUT

Parameter	Min	Typ	Max	Unit
Input Voltage (RMS Values Assume Sine Wave Input)				
LINE_IN, AUX, CD, VIDEO, PHONE_IN, PC_BEEP		1		V rms
		2.83		V p-p
MIC with +20 dB Gain (M20 = 1)		0.1		V rms
		0.283		V p-p
MIC with 0 dB Gain (M20 = 0)		1		V rms
		2.83		V p-p
Input Impedance*		20		kΩ
Input Capacitance*		5	7.5	pF

MASTER VOLUME

Parameter	Min	Typ	Max	Unit
Step Size (0 dB to –94.5 dB); LINE_OUT_L, LINE_OUT_R		1.5		dB
Output Attenuation Range Span*		–94.5		dB
Step Size (0 dB to –46.5 dB); MONO_OUT		1.5		dB
Output Attenuation Range Span*		–46.5		dB
Mute Attenuation of 0 dB Fundamental*			80	dB

PROGRAMMABLE GAIN AMPLIFIER—ADC

Parameter	Min	Typ	Max	Unit
Step Size (0 dB to 22.5 dB)		1.5		dB
PGA Gain Range Span		22.5		dB

ANALOG MIXER—INPUT GAIN/AMPLIFIERS/ATTENUATORS

Parameter	Min	Typ	Max	Unit
Signal-to-Noise Ratio (SNR)				
CD to LINE_OUT		90		dB
Other to LINE_OUT		90		dB
Step Size (+12 dB to –34.5 dB): (All Steps Tested)				
MIC, LINE_IN, AUX, CD, VIDEO, PHONE_IN, DAC		1.5		dB
Input Gain/Attenuation Range: MIC, LINE, AUX, CD, VIDEO, PHONE_IN, DAC		–46.5		dB
Step Size (0 dB to –45 dB): (All Steps Tested) PC_BEEP		3.0		dB
Input Gain/Attenuation Range: PC_BEEP		–45		dB

*Guaranteed, not tested.
Specifications subject to change without notice.

DIGITAL DECIMATION AND INTERPOLATION FILTERS*

Parameter	Min	Typ	Max	Unit
Passband	0		$0.4 \times F_S$	Hz
Passband Ripple			±0.09	dB
Transition Band	$0.4 \times F_S$		$0.6 \times F_S$	Hz
Stopband	$0.6 \times F_S$		∞	Hz
Stopband Rejection	–74			dB
Group Delay			$12/F_S$	sec
Group Delay Variation Over Passband			0.0	µs

ANALOG-TO-DIGITAL CONVERTERS

Parameter	Min	Typ	Max	Unit
Resolution		16		Bits
Total Harmonic Distortion (THD)			0.02	%
			–74	dB
Dynamic Range (–60 dB Input THD+N Referenced to Full Scale, A-Weighted)		87		dB
Signal-to-Intermodulation Distortion* (CCIF Method)		85		dB
ADC Crosstalk*				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–100	–90	dB
LINE_IN to Other		–90	–85	dB
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
ADC Offset Error			±10.5	mV

DIGITAL-TO-ANALOG CONVERTERS

Parameter	Min	Typ	Max	Unit
Resolution		16		Bits
Total Harmonic Distortion (THD) LINE_OUT, LNLVL_OUT			0.02	%
			–74	dB
Dynamic Range (–60 dB Input THD+N Referenced to Full Scale, A-Weighted)		90		dB
Signal-to-Intermodulation Distortion* (CCIF Method)		85		dB
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)		±10		%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.7	dB
DAC Crosstalk* (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)			–80	dB
Total Audible Out-of-Band Energy (Measured from $0.6 \times F_S$ to 20 kHz)*		–40		dB

ANALOG OUTPUT

Parameter	Min	Typ	Max	Unit
Full-Scale Output Voltage		1		V rms
(LINE_OUT, LNLVL_OUT)		2.83		V p-p
Output Impedance*			500	Ω
External Load Impedance*	10			kΩ
Output Capacitance*		15		pF
External Load Capacitance			100	pF
V_{REF}	2.0	2.2	2.5	V
V_{REF_OUT}		2.2		V
Mute Click (Muted Output Minus Unmuted Midscale DAC Output)		±5		mV

*Guaranteed, not tested.
Specifications subject to change without notice.

AD1881A–SPECIFICATIONS

STATIC DIGITAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
High Level Input Voltage (V_{IH}): Digital Inputs	$0.65 \times DV_{DD}$			V
Low Level Input Voltage (V_{IL})			$0.35 \times DV_{DD}$	V
High Level Output Voltage (V_{OH}), I_{OH} = –0.5 mA	$0.9 \times DV_{DD}$			V
Low Level Output Voltage (V_{OL}), I_{OL} = +0.5 mA			$0.1 \times DV_{DD}$	V
Input Leakage Current	–10		+10	µA
Output Leakage Current	–10		+10	µA

POWER SUPPLY

Parameter	Min	Typ	Max	Unit
Power Supply Range – Analog	4.75		5.25	V
Power Supply Range – Digital (3.3 V)	3.0		3.6	V
Power Dissipation – 5 V/3.3 V		280		mW
Analog Supply Current – 5 V		40		mA
Digital Supply Current – 3.3 V		23		mA
Power Supply Rejection (100 mV p-p Signal @ 1 kHz)* (At Both Analog and Digital Supply Pins, Both ADCs and DACs)		40		dB

CLOCK SPECIFICATIONS*

Parameter	Min	Typ	Max	Unit
Input Clock Frequency		24.576		MHz
Recommended Clock Duty Cycle	45	50	55	%

POWER-DOWN MODE

Parameter	Set Bits	DV_{DD} (3.3 V) Typ	AV_{DD} (5 V) Typ	Unit
ADC	PR0	17	30	mA
DAC	PR1	17	26	mA
ADC and DAC	PR1, PR0	4	20	mA
ADC + DAC + Mixer (Analog CD On)	LPMIX, PR1, PR0	4	12	mA
Mixer	PR2	20	18	mA
ADC + Mixer	PR2, PR0	17	12	mA
DAC + Mixer	PR2, PR1	17	8	mA
ADC + DAC + Mixer	PR2, PR1, PR0	4	2	mA
Analog CD Only (AC-Link On)	LPMIX, PR5, PR1, PR0	4	12	mA
Analog CD Only (AC-Link Off)	LPMIX, PR1, PR0, PR4, PR5	0	12	mA
Standby	PR5, PR4, PR3, PR2, PR1, PR0	0	0.1	mA

*Guaranteed, not tested.
Specifications subject to change without notice.

TIMING PARAMETERS[1] (GUARANTEED OVER OPERATING TEMPERATURE RANGE)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RESET}}$ Active Low Pulsewidth	t_{RST_LOW}	50			ns
$\overline{\text{RESET}}$ Inactive to BIT_CLK Startup Delay	$t_{RST2CLK}$		833		µs
SYNC Active High Pulsewidth	t_{SYNC_HIGH}	80			ns
SYNC Low Pulsewidth	t_{SYNC_LOW}		19.5		µs
SYNC Inactive to BIT_CLK Startup Delay	$t_{SYNC2CLK}$	162.8			ns
BIT_CLK Frequency			12.288		MHz
BIT_CLK Period	t_{CLK_PERIOD}		81.4		ns
BIT_CLK Output Jitter[2]				750	ps
BIT_CLK High Pulsewidth	t_{CLK_HIGH}	36.62	40.69	44.76	ns
BIT_CLK Low Pulsewidth	t_{CLK_LOW}	36.62	40.69	44.76	ns
SYNC Frequency			48.0		kHz
SYNC Period	t_{SYNC_PERIOD}		20.8		µs
Setup to Falling Edge of BIT_CLK	t_{SETUP}	5	2.5		ns
Hold from Falling Edge of BIT_CLK	t_{HOLD}	5			ns
BIT_CLK Rise Time	$t_{RISECLK}$	2	4	10	ns
BIT_CLK Fall Time	$t_{FALLCLK}$	2	4	10	ns
SYNC Rise Time	$t_{RISESYNC}$	2	4	10	ns
SYNC Fall Time	$t_{FALLSYNC}$	2	4	10	ns
SDATA_IN Rise Time	$t_{RISEDIN}$	2	4	10	ns
SDATA_IN Fall Time	$t_{FALLDIN}$	2	4	10	ns
SDATA_OUT Rise Time	$t_{RISEDOUT}$	2	4	10	ns
SDATA_OUT Fall Time	$t_{FALLDOUT}$	2	4	10	ns
End of Slot 2 to BIT_CLK, SDATA_IN Low	t_{S2_PDOWN}	0		10	ms
Setup to Trailing Edge of $\overline{\text{RESET}}$ (Applies to SYNC, SDATA_OUT)	$t_{SETUP2RST}$	15			ns
Rising Edge of $\overline{\text{RESET}}$ to HI-Z Delay (ATE Test Mode)	t_{OFF}			25	ns
Propagation Delay				15	ns
$\overline{\text{RESET}}$ Rise Time				50	ns

NOTES

[1]Guaranteed, not tested.

[2]Output jitter is directly dependent on crystal input jitter.

Specifications subject to change without notice.

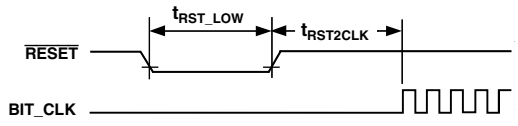


Figure 1. Cold Reset

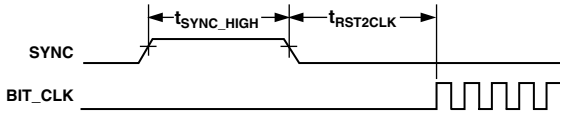


Figure 2. Warm Reset

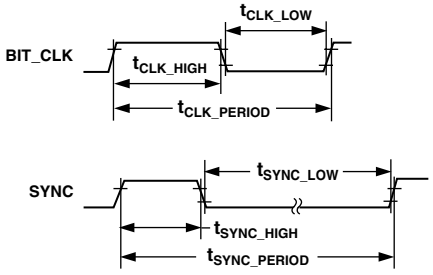


Figure 3. Clock Timing

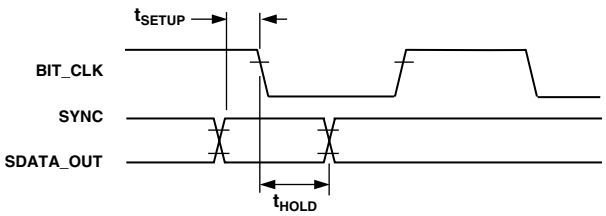


Figure 4. Data Setup and Hold

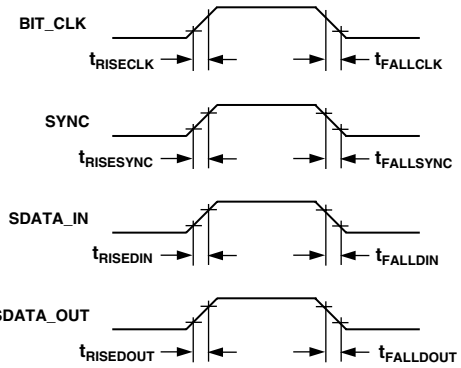


Figure 5. Signal Rise and Fall Time

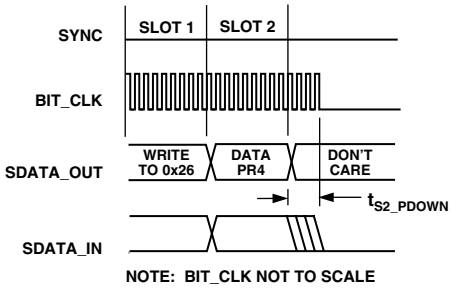


Figure 6. AC Link Low Power Mode Timing

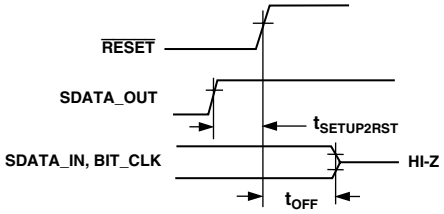


Figure 7. ATE Test Mode

ABSOLUTE MAXIMUM RATINGS*

Parameter	Min	Max	Unit
Power Supplies			
Digital (V_{DD})	–0.3	+3.6	V
Analog (V_{CC})	–0.3	+6.0	V
Analog Input Voltage (Signal Pins)	–0.3	V_{CC} + 0.3	V
Digital Input Voltage (Signal Pins)	–0.3	V_{DD} + 0.3	V
Ambient Temperature (Operating)	0	+70	°C
Storage Temperature	–65	+150	°C

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1881AJST	0°C to 70°C	48-Lead LQFP	ST-48

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$

T_{CASE} = Case Temperature in °C

P_D = Power Dissipation in W

θ_{CA} = Thermal Resistance (Case-to-Ambient)

θ_{JA} = Thermal Resistance (Junction-to-Ambient)

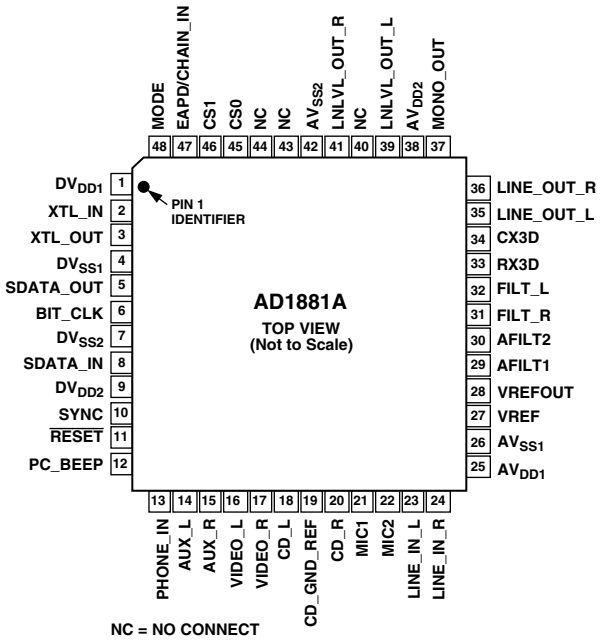
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
LQFP	76.2°C/W	17°C/W	59.2°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1881A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
48-Lead LQFP



PIN FUNCTION DESCRIPTIONS

Digital I/O

Pin Name	LQFP	I/O	Description
XTL_IN	2	I	Crystal (or Clock) Input, 24.576 MHz.
XTL_OUT	3	O	Crystal Output.
SDATA_OUT	5	I	AC-Link Serial Data Output, AD1881A Input Stream.
BIT_CLK	6	O	AC-Link Bit Clock. 12.288 MHz Serial Data Clock. Daisy Chain Output Clock.
SDATA_IN	8	O	AC-Link Serial Data Input. AD1881A Output Stream.
SYNC	10	I	AC-Link Frame Sample Sync 48 kHz Fixed Rate.
$\overline{\text{RESET}}$	11	I	AC-Link Reset. AD1881A Master H/W Reset.

Miscellaneous Connections

Pin Name	LQFP	I/O	Description
CS0	45	I	Chip Select 0.
CS1	46	I	Chip Select 1.
EAPD	47	O	External Amp Power-Down Control Signal, Default LO, Active HI
MODE	48	I	MODE Select.

Analog I/O

These signals connect the AD1881A component to analog sources and sinks, including microphones and speakers.

Pin Name	LQFP	I/O	Description
PC_BEEP	12	I	PC Beep. PC Speaker Beep Passthrough.
PHONE_IN	13	I	Phone. From Telephony Subsystem Speakerphone or Handset.
AUX_L	14	I	Auxiliary Input Left Channel.
AUX_R	15	I	Auxiliary Input Right Channel.
VIDEO_L	16	I	Video Audio Left Channel.
VIDEO_R	17	I	Video Audio Right Channel.
CD_L	18	I	CD Audio Left Channel.
CD_GND_REF	19	I	CD Audio Analog Ground Reference for Pseudo-Differential CD Input.
CD_ R	20	I	CD Audio Right Channel.
MIC1	21	I	Microphone 1. Desktop Microphone Input.
MIC2	22	I	Microphone 2. Second Microphone Input.
LINE_IN_L	23	I	Line In Left Channel.
LINE_IN_R	24	I	Line In Right Channel.
LINE_OUT_L	35	O	Line Out Left Channel.
LINE_OUT_R	36	O	Line Out Right Channel.
MONO_OUT	37	O	Monaural Output to Telephony Subsystem Speakerphone.
LNLVL_OUT_L	39	O	Line-Level Output Left Channel.
LNLVL_OUT_R	41	O	Line-Level Output Right Channel.

Filter/Reference

These signals are connected to resistors, capacitors, or specific voltages.

Pin Name	LQFP	I/O	Description
VREF	27	O	Voltage Reference Filter.
VREFOUT	28	O	Voltage Reference Output 5 mA Drive (Intended for MIC Bias).
AFILT1	29	O	Antialiasing Filter Capacitor—ADC Right Channel.
AFILT2	30	O	Antialiasing Filter Capacitor—ADC Left Channel.
FILT_R	31	O	AC-Coupling Filter Capacitor—ADC Right Channel.
FILT_L	32	O	AC-Coupling Filter Capacitor—ADC Left Channel.
RX3D	33	O	3D PHAT Stereo Enhancement—Capacitor.
CX3D	34	I	3D PHAT Stereo Enhancement—Capacitor.

Power and Ground Signals

Pin Name	LQFP	Type	Description
DV_{DD1}	1	I	Digital V_{DD} 3.3 V
DV_{SS1}	4	I	Digital GND
DV_{SS2}	7	I	Digital GND
DV_{DD2}	9	I	Digital V_{DD} 3.3 V
AV_{DD1}	25	I	Analog V_{DD} 5.0 V
AV_{SS1}	26	I	Analog GND
AV_{DD2}	38	I	Analog V_{DD} 5.0 V
AV_{SS2}	42	I	Analog GND

No Connects

Pin Name	LQFP	Type	Description
NC	40		No Connect
NC	43		No Connect
NC	44		No Connect

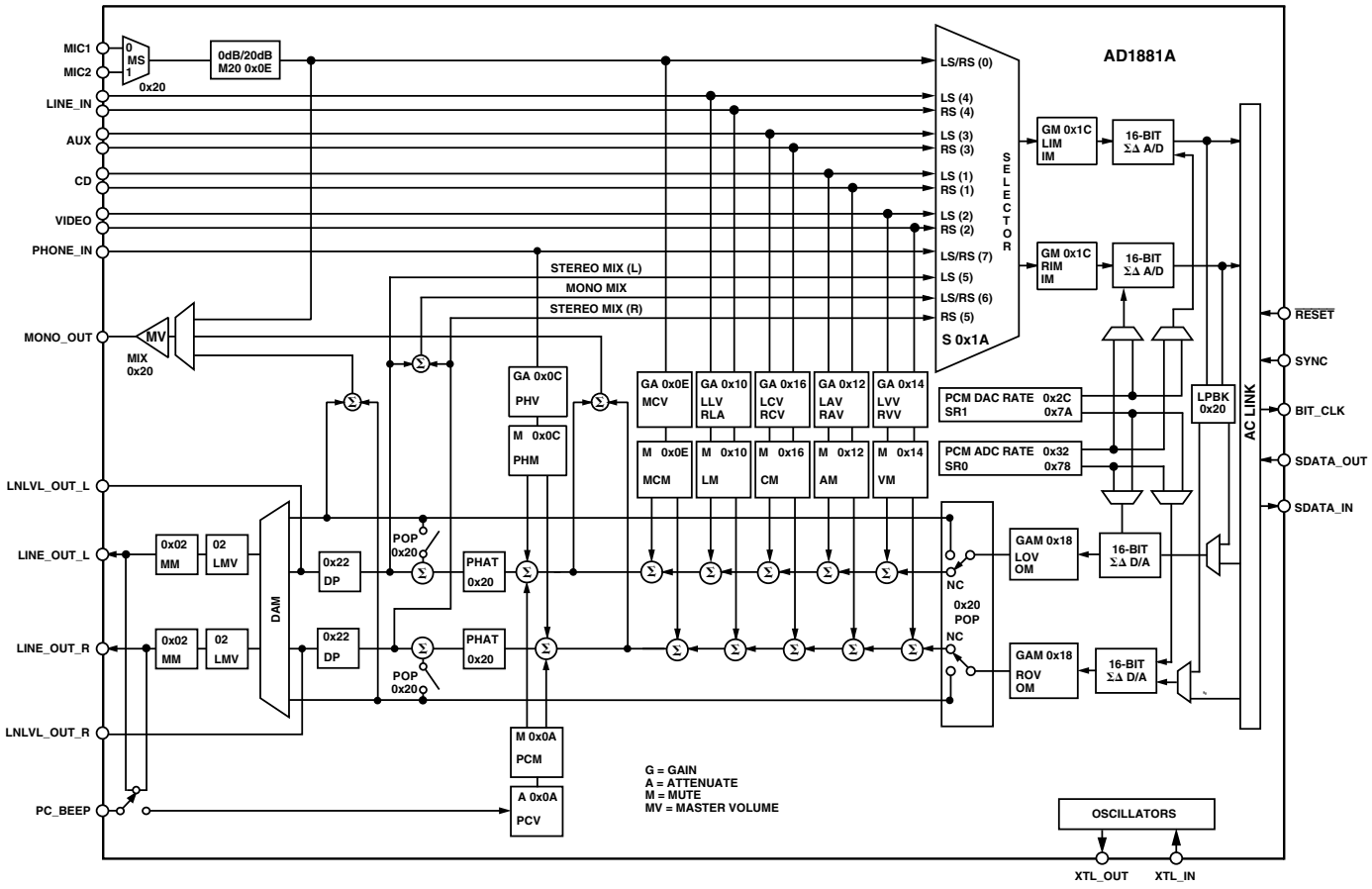


Figure 8. Block Diagram Register Map

PRODUCT OVERVIEW

The AD1881A meets the *Audio Codec '97 2.0 and 2.1 Extensions.* In addition, the AD1881A SoundMAX Codec is designed to meet all requirements of the *Audio Codec '97, Component Specification*, Revision 1.03, © 1996, Intel Corporation, found at *www.Intel.com*. The AD1881A also includes some other Codec enhanced features such as the built-in PHAT Stereo 3D enhancement.

The AD1881A is an analog front end for high performance PC audio applications. The AC'97 architecture defines a 2-chip audio solution comprising a digital audio controller, plus a high quality analog component that includes Digital-to-Analog Converters (DACs), Analog-to-Digital Converters (ADCs), mixer and I/O.

The main architectural features of the AD1881A are the high quality analog mixer section, two channels of ΣΔ ADC conversion, two channels of ΣΔ DAC conversion with Data Direct Scrambling (D^2S) rate generators. The AD1881A's left channel ADC and DAC are compatible for modem applications supporting irrational sample rates and modem filtering requirements.

FUNCTIONAL DESCRIPTION

This section overviews the functionality of the AD1881A and is intended as a general introduction to the capabilities of the device. Detailed reference information may be found in the descriptions of the Indexed Control Registers.

Analog Inputs

The Codec contains a stereo pair of ΣΔ ADCs. Inputs to the ADC may be selected from the following analog signals: telephony (PHONE_IN), mono microphone (MIC1 or MIC2), stereo line (LINE_IN), auxiliary line input (AUX), stereo CD ROM (CD), stereo audio from a video source (VIDEO) and post-mixed stereo or mono line output (LINE_OUT).

Analog Mixing

PHONE_IN, MIC1 or MIC2, LINE_IN, AUX, CD and VIDEO can be mixed in the analog domain with the stereo output from the DACs. Each channel of the stereo analog inputs may be independently gained or attenuated from +12 dB to –34.5 dB in 1.5 dB steps. The summing path for the mono inputs (PHONE_IN, MIC1, and MIC2 to LINE_OUT) duplicates mono channel data on both the left and right LINE_OUT. Additionally, the PC attention signal (PC_BEEP) may be mixed with the line output. A switch allows the output of the DACs to bypass the PHAT Stereo 3D enhancement.

Digital Audio Mode

The AD1881A is designed with a Digital Audio Mode (DAM) that allows mixing of all analog inputs independent of the DAC output signal path. Mixed analog input signals may be sent to the ADCs for processing by the controller or the host, and may be used during simultaneous capture and playback at different sample rates.

Analog-to-Digital Signal Path

The selector sends left and right channel information to the programmable gain amplifier (PGA). The PGA following the selector allows independent gain control for each channel entering the ADC from 0 dB to +22.5 dB in 1.5 dB steps. Each channel of the ADC is independent, and can process left and right channel data at different sample rates.

Sample Rates and D^2S

The AD1881A default mode sets the Codec to operate at 48 kHz sample rates. The converter pairs may process left and right channel data at different sample rates. The AD1881A sample rate generator allows the Codec to instantaneously change and process sample rates from 8 kHz to 48 kHz with a resolution of 1 Hz. The in-band integrated noise and distortion artifacts introduced by rate conversions are below –90 dB. The AD1881A uses a 4-bit D/A structure and Data Directed Scrambling (D^2S) to enhance noise immunity on motherboards and in PC enclosures, and to suppress idle tones below the device's quantization noise floor. The D^2S process pushes noise and distortion artifacts caused by errors in the multibit DAC to frequencies beyond the auditory response of the human ear and then filters them.

Digital-to-Analog Signal Path

The analog output of the DAC may be gained or attenuated from +12 dB to –34.5 dB in 1.5 dB steps, and summed with any of the analog input signals. The summed analog signal enters the Master Volume stage where each channel of the mixer output may be attenuated from 0 dB to –94.5 dB in 1.5 dB steps or muted.

Line-Level Outputs

The AD1881A offers a true line-level output for notebook docking station and home theater applications. The line-level output does not change with master volume settings.

Host-Based Echo Cancellation Support

The AD1881A supports time correlated I/O data format by presenting MIC data on the left channel of the ADC and the mono summation of left and right output on the right channel. The ADC is splittable; left and right ADC data can be sampled at different rates.

Power Management Modes

The AD1881A is designed to meet ACPI power consumption requirements through flexible power management control of all internal resources.

Indexed Control Registers

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0410h
02h	Master Volume	MM	X	LMV5	LMV4	LMV3	LMV2	LMV1	LMV0	X	X	RMV5	RMV4	RMV3	RMV2	RMV1	RMV0	8000h
04h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
06h	Master Volume Mono	MMM	X	X	X	X	X	X	X	X	X	X	MMV 4	MMV 2	MMV 2	MMV 1	MMV 0	8000h
08h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
0Ah	PC Beep Volume	PCM	X	X	X	X	X	X	X	X	X	X	PCV3	PCV2	PCV1	PCV0	X	8000h
0Ch	Phone In Volume	PHM	X	X	X	X	X	X	X	X	X	X	PHV4	PHV3	PHV2	PHV1	PHV0	8008h
0Eh	MIC Volume	MCM	X	X	X	X	X	X	X	X	M20	X	MCV4	MCV3	MCV2	MCV1	MCV0	8008h
10h	Line In Volume	LM	X	X	LLV4	LLV3	LLV2	LLV1	LLV0	X	X	X	RLV4	RLV3	RLV2	RLV1	RLV0	8808h
12h	CD Volume	CVM	X	X	LCV4	LCV3	LCV2	LCV1	LCV0	X	X	X	RCV4	RCV3	RCV2	RCV1	RCV0	8808h
14h	Video Volume	VM	X	X	LVV4	LVV3	LVV2	LVV1	LVV0	X	X	X	RVV4	RVV3	RVV2	RVV1	RVV0	8808h
16h	Aux Volume	AM	X	X	LAV4	LAV3	LAV2	LAV1	LAV0	X	X	X	RAV4	RAV3	RAV2	RAV1	RAV0	8808h
18h	PCM Out Vol	OM	X	X	LOV4	LOV3	LOV2	LOV1	LOV0	X	X	X	ROV4	ROV3	ROV2	ROV1	ROV0	8808h
1Ah	Record Select	X	X	X	X	X	LS2	LS1	LS0	X	X	X	X	X	RS2	RS1	RS0	0000h
1Ch	Record Gain	IM	X	X	X	LIM3	LIM2	LIM1	LIM0	X	X	X	X	RIM3	RIM2	RIM1	RIM0	8000h
1Eh	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
20h	General Purpose	POP	X	3D	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	DP3	DP2	DP1	DP0	0000h
26h	Power-Down Cntrl/Stat	EAPD	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Xh
28h	Extended Audio ID	ID1	ID0	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0001h
2Ah	Extended Audio Stat/Ctrl	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0000h
2Ch/ (7Ah)*	PCM DAC Rate (SR1)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h / (78h)*	PCM ADC Rate (SR0)	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
34h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
5ah 70h	Vendor Reserved**	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..
72h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
74h	Serial Configuration	SLOT 16	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	7X0Xh
76h	Misc. Control Bits	DAC Z	LPMI X	X	DAM	DMS	DLSR	X	ALSR	MOD EN	SRX 10D7	SRX 8D7	X	X	DRSR	X	ARSR	0404h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4144h
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5348h

NOTES
All registers not shown and bits containing an X are assumed to be reserved.
Odd register addresses are aliased to the next lower even address.
Reserved registers should not be written.
Zeros should be written to reserved bits.
*Indicates Aliased register for AD1819, AD1819A backward compatibility.
**Vendor Reserved registers should not be written.

Reset (Index 00h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0410h

Note: Writing any value to this register performs a register reset, which causes all registers to revert to their default values (except 74h, which forces the serial configuration). Reading this register returns the ID code of the part and a code for the type of 3D Stereo Enhancement.

ID[9:0] Identify Capability. The ID decodes the capabilities of AD1881A based on the following:

Bit = 1	Function	AD1881A
ID0	Dedicated MIC PCM In Channel	0
ID1	Modem Line Codec Support	0
ID2	Bass and Treble Control	0
ID3	Simulated Stereo (Mono to Stereo)	0
ID4	Headphone Out/True Line-Level Out	1
ID5	Loudness (Bass Boost) Support	0
ID6	18-Bit DAC Resolution	0
ID7	20-Bit DAC Resolution	0
ID8	18-Bit ADC Resolution	0
ID9	20-Bit ADC Resolution	0

SE[4:0] Stereo Enhancement. The 3D stereo enhancement identifies the Analog Devices 3D stereo enhancement.

Master Volume Registers (Index 02h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	Master Volume	MM	X	LMV5	LMV4	LMV3	LMV2	LMV1	LMV0	X	X	RMV5	RMV4	RMV3	RMV2	RMV1	RMV0	8000h

RMV[5:0] Right Master Volume Control. The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of –94.5 dB.

LMV[5:0] Left Master Volume Control. The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of –94.5 dB.

MM Master Volume Mute. When this bit is set to "1," the channel is muted.

MM	xMV5 . . . xMV0	Function
0	00 0000	0 dB Attenuation
0	01 1111	–46.5 dB Attenuation
0	11 1111	–94.5 dB Attenuation
1	xx xxxx	–∞ dB Attenuation

Master Volume Mono (Index 06h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
06h	Master Volume Mono	MMM	X	X	X	X	X	X	X	X	X	X	MMV4	MMV3	MMV2	MMV1	MMV0	8000h

MMV[4:0] Mono Master Volume Control. The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of –46.5 dB.

MMM Mono Master Volume Mute. When this bit is set to "1," the channel is muted.

PC Beep Register (Index 0Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ah	PC_BEEP Volume	PCM	X	X	X	X	X	X	X			X	PCV3	PCV2	PCV1	PCV0	X	8000h

PCV[3:0] PC Beep Volume Control. The least significant bit represents 3 dB attenuation. This register controls the output from 0 dB to a maximum attenuation of –45 dB. The PC Beep is routed to Left and Right Line outputs even when the $\overline{\text{RESET}}$ pin is asserted. This is so that Power on Self-Test (POST) codes can be heard by the user in case of a hardware problem with the PC.

PCM PC Beep Mute. When this bit is set to "1," the channel is muted.

PCM	PCV3 . . . PCV0	Function
0	0000	0 dB Attenuation
0	1111	–45 dB Attenuation
1	xxxx	–∞ dB Attenuation

Phone Volume (Index 0Ch)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ch	Phone Volume	PHM	X	X	X	X	X	X	X			X	PHV4	PHV3	PHV2	PHV1	PHV0	8008h

PHV[4:0] Phone Volume. Allows setting the Phone Volume Attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

PHM Phone Mute. When this bit is set to "1," the channel is muted.

MIC Volume (Index 0Eh)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Eh	Mic Volume	MCM	X	X	X	X	X	X	X	X	M20	X	MCV4	MCV3	MCV2	MCV1	MCV0	8008h

MCV[4:0] MIC Volume Gain. Allows setting the MIC Volume attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

M20 Microphone 20 dB Gain Block
0 = Disabled; Gain = 0 dB.
1 = Enabled; Gain = 20 dB.

MCM MIC Mute. When this bit is set to "1," the channel is muted.

Line In Volume (Index 10h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	Line InVolume	LM	X	X	LLV4	LLV3	LLV2	LLV1	LLV0	X	X	X	RLV4	RLV3	RLV2	RLV1	RLV0	8808h

RLV[4:0] Right Line In Volume. Allows setting the Line In right channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LLV[4:0] Line In Volume Left. Allows setting the Line In left channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LM Line In Mute. When this bit is set to "1," the channel is muted.

CD Volume (Index 12h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
12h	CD Volume	CVM	X	X	LCV4	LCV3	LCV2	LCV1	LCV0	X	X	X	RCV4	RCV3	RCV2	RCV1	RCV0	8808h

RCV[4:0] Right CD Volume. Allows setting the CD right channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LCV[4:0] Left CD Volume. Allows setting the CD left channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

CVM CD Volume Mute. When this bit is set to "1," the channel is muted.

Video Volume (Index 14h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
14h	Video Volume	VM	X	X	LVV4	LVV3	LVV2	LVV1	LVV0	X	X	X	RVV4	RVV3	RVV2	RVV1	RVV0	8808h

RVV[4:0] Right Video Volume. Allows setting the Video right channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LVV[4:0] Left Video Volume. Allows setting the Video left channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

VM Video Mute. When this bit is set to "1," the channel is muted.

AUX Volume (Index 16h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
16h	Aux Volume	AM	X	X	LAV4	LAV3	LAV2	LAV1	LAV0	X	X	X	RAV4	RAV3	RAV2	RAV1	RAV0	8808h

RAV[4:0] Right Aux. Volume. Allows setting the Aux right channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LAV[4:0] Left Aux. Volume. Allows setting the Aux left channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

AM Aux. Mute. When this bit is set to "1," the channel is muted.

PCM Out Volume (Index 18h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	PCM Out Volume	OM	X	X	LOV4	LOV3	LOV2	LOV1	LOV0	X	X	X	ROV4	ROV3	ROV2	ROV1	ROV0	8808h

ROV[4:0] Right PCM Out Volume. Allows setting the PCM right channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

LOV[4:0] Left PCM Out Volume. Allows setting the PCM left channel attenuator in 32 steps. The LSB represents 1.5 dB, and the range is +12 dB to –34.5 dB. The default value is 0 dB, mute enabled.

OM PCM Out Volume Mute. When this bit is set to "1," the channel is muted.

Volume Table (Index 0Ch to 18h)

MM	x4 . . . x0	Function
0	00000	+12 dB Gain
0	01000	0 dB Gain
0	11111	–34.5 dB Gain
1	xxxxx	–∞ dB Gain

Record Select Control Register (Index 1Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah	Record Select	X	X	X	X	X	LS2	LS1	LS0	X	X	X	X	X	RS2	RS1	RS0	0000h

RS[2:0] Right Record Select

LS[2:0] Left Record Select.

Used to select the record source independently for right and left. See table for legend.

The default value is 0000h, which corresponds to MIC in.

RS2 . . . RS0	Right Record Source
0	MIC
1	CD_R
2	VIDEO_R
3	AUX_R
4	LINE_IN_R
5	Stereo Mix (R)
6	Mono Mix
7	PHONE_IN

LS2 . . . LS0	Left Record Source
0	MIC
1	CD_L
2	VIDEO_L
3	AUX_L
4	LINE_IN_L
5	Stereo Mix (L)
6	Mono Mix
7	PHONE_IN

Record Gain (Index 1Ch)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	Record Gain	IM	X	X	X	LIM3	LIM2	LIM1	LIM0	X	X	X	X	RIM3	RIM2	RIM1	RIM0	8000h

RIM[3:0] Right Input Mixer Gain Control. Each LSB represents 1.5 dB, 0000 = 0 dB and the range is 0 dB to +22.5 dB.

LIM[3:0] Left Input Mixer Gain Control. Each LSB represents 1.5 dB, 0000 = 0 dB and the range is 0 dB to +22.5 dB.

IM Input Mute.
0 = Unmuted,
1 = Muted or –∞ dB gain.

IM	xIM3 . . . xIM0	Function
0	1111	+22.5 dB Gain
0	0000	0 dB Gain
1	xxxxx	–∞ dB Gain

General Purpose Register (Index 20h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	General Purpose	POP	X	3D	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h

Note: This register should be read before writing to generate a mask for only the bit(s) that need to be changed. The function default value is 0000h which is all off.

LPBK Loopback Control. ADC/DAC Digital Loopback Mode

MS MIC Select
0 = MIC1.
1 = MIC2.

MIX Mono Output Select
0 = Mix.
1 = MIC.

3D 3D PHAT Stereo Enhancement
0 = PHAT Stereo is off.
1 = PHAT Stereo is on.

POP PCM Output Path and Mute. The POP bit controls the optional PCM out 3D bypass path (the pre- and post-3D PCM out paths are mutually exclusive).
0 = pre-3D.
1 = post-3D.

3D Control Register (Index 22h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	DP3	DP2	DP1	DP0	0000h

DP[2:0] Depth Control. Sets 3D "Depth" PHAT Stereo enhancement according to table below.

DP3 . . . DP0	Depth
0000	0%
0001	6.67%
.	.
.	.
1110	93.33%
1111	100%

Subsection Ready Register (Index 26h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	Power-Down Cntrl/Stat	EAPD	X	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	N/A

Note: The ready bits are read only, writing to REF, ANL, DAC, ADC will have no effect. These bits indicate the status for the AD1881A subsections. If the bit is a one, then that subsection is "*ready*." Ready is defined as the subsection able to perform in its nominal state.

ADC — ADC section ready to transmit data.

DAC — DAC section ready to accept data.

ANL — Analog gain, attenuators and mute blocks, and mixers ready.

REF — Voltage References, VREF and VREFOUT up to nominal level.

PR[5:0] — AD1881A Power-Down Modes. The first three bits are to be used individually rather than in combination with each other. The last bit PR3 can be used in combination with PR2 or by itself. The mixer and reference cannot be powered down via PR3 unless the ADCs and DACs are also powered down. Nothing else can be powered up until the reference is up.

PR5 has no effect unless all ADCs, DACs, and the AC-Link are powered down. The reference and the mixer can either be up or down, but all power-up sequences must be allowed to run to completion before PR5 and PR4 are both set.

In multiple-codec systems, the master codec's PR5 and PR4 bits control the slave codec. PR5 is also effective in the slave codec if the master's PR5 bit is clear, but the PR4 bit has no effect except to enable or disable PR5.

EAPD — External Audio Amp Power Down. Available when programmed as an AC'97 codec.
0 = Pin 47 set to LO state (default).
1 = Pin 47 set to HI state.

Power-Down State	PR5	PR4	PR3	PR2	PR1	PR0
ADC Power-Down	0	0	0	0	0	1
DAC Power-Down	0	0	0	0	1	0
ADC and DAC Power-Down	0	0	0	0	1	1
Mixer Power-Down	0	0	0	1	0	0
ADC + Mixer Power-Down	0	0	0	1	0	1
DAC + Mixer Power-Down	0	0	0	1	1	0
ADC + DAC + Mixer Power-Down	0	0	0	1	1	1
Standby	1	1	1	1	1	1

Extended Audio ID Register (Index 28h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	ID1	ID0	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0000h

Note: The Extended Audio ID is a read only register.

VRA — Variable Rate Audio. VRA = 1 enables Variable Rate Audio.

ID[1:0] — ID1, ID0 is a 2-bit field that indicates the codec configuration: Primary is 00; Secondary is 01, 10, or 11.

Extended Audio Status and Control Register (Index 2Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ah	Extended Audio St/Ctrl	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0000h

Note: The Extended Audio Status and Control Register is a read/write register that provides status and control of the extended audio features.

VRA Variable Rate Audio. VRA = 1 enables Variable Rate Audio mode (sample rate control registers and SLOTREQ signaling.

PCM DAC Rate Register (Index 2Ch)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ch/(7Ah)	PCM DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Note: 2Ch is an alias for 7Ah. The VRA bit in register 2Ah must be set for the alias to work; if a zero is written to VRA, both sample rates are reset to 48k.

SR[15:0] Writing to this register allows programming of the sampling frequency from 8 kHz (1B80h) to 48 kHz (BB80h) in 1 Hz increments. Programming a value outside of the range 7040 Hz (1b80h) to 48000 Hz (bb80h) causes the codec to saturate to 48 kHz if a rate greater than 48 kHz is programmed or to 7.040 kHz if a rate less than 7.040 kHz is programmed. For all rates, if the value written to the register is supported, that value will be echoed back when read, otherwise the closest rate supported is returned.

PCM ADC Rate Register (Index 32h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
32h/(78h)	PCM ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Note: 32h is an alias for 78h. The VRA bit in register 2Ah must be set for the alias to work; if a zero is written to VRA, both sample rates are reset to 48k.

SR[15:0] Writing to this register allows programming of the sampling frequency from 8 kHz (1B80) to 48 kHz (BB80h) in 1 Hz increments. Programming a value outside of the range 7040 Hz (1b80h) to 48000 Hz (bb80h) causes the codec to saturate to 48 kHz if a rate greater than 48 kHz is programmed, or to 7.040 kHz if a rate less than 7.040 kHz is programmed. For all rates, if the value written to the register is supported, that value will be echoed back when read, otherwise the closest rate supported is returned.

Serial Configuration (Index 74h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
74h	Serial Configuration	SLOT 16	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	7x0xh

Note: This register is not reset when the reset register (register 00h) is written.

SLOT16 Enable 16-bit slots.

DRQEN and DxRQx are retained only for compatibility with the AD1819. New controller designs should use the VRA bit in register 2Ah and the request bits in the status address slot instead.

If your system uses only a single AD1881A, you can ignore the register mask and the slave 1/slave 2 request bits. If you write to this register, write ones to all of the register mask bits.

SLOT16 makes all AC Link slots 16 bits in length, formatted into 16 slots.

Miscellaneous Control Bits (Index 76h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
76h	Misc Control Bits	DACZ	LPMIX	X	DAM	DMS	DLSR	X	ALSR	MODEN	SRX10D7	SRX8D7	X	X	DRSR	X	ARSR	0404h

ARSR ADC right sample generator select
0 = SR0 Selected (32h)
1 = SR1 Selected (2Ch).

DRSR DAC right sample generator select
0 = SR0 Selected (32h)
1 = SR1 Selected (2Ch).

SRX8D7 Multiply SR1 rate by 8/7.

SRX10D7 Multiply SR1 rate by 10/7. SRX10D7 and SRX8D7 are mutually exclusive; SRX10D7 has priority if both are set.

MODEN Modem filter enable (left channel only). Change only when DACs are powered down.

ALSR ADC left sample generator select
0 = SR0 Selected (32h)
1 = SR1 Selected (2Ch).

DLSR DAC left sample generator select
0 = SR0 Selected (32h)
1 = SR1 Selected (2Ch).

DMS Digital Mono Select.
0 = Mixer
1 = Left DAC and Right DAC.

DAM Digital Audio Mode. DAC Outputs bypass analog mixer and sent directly to the codec output.

LPMIX Low Power Mixer. Keeps CD to LINE_OUT alive for notebook applications.

DACZ Zero fill (vs. repeat) if DAC is starved for data.

Sample Rate 0 (Index 78h)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
78h	Sample Rate 0	SR015	SR014	SR013	SR012	SR011	SR010	SR09	SR08	SR07	SR06	SR05	SR04	SR03	SR02	SR01	SR00	BB80H

Note: 32h is an alias for 78h. The VRA bit in register 2Ah must be set for the alias to work; if a zero is written to VRA then both sample rates are reset to 48k.

SR0[15:0] Writing to this register allows the user to program the sampling frequency from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hertz increments. Programming a value greater than 48 kHz or less than 7 kHz may cause unpredictable results.

Sample Rate 1 (Index 7Ah)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ah	Sample Rate 1	SR115	SR114	SR113	SR112	SR111	SR110	SR19	SR18	SR17	SR16	SR15	SR14	SR13	SR12	SR11	SR10	BB80h

Note: 2Ch is an alias for 7Ah. The VRA bit in register 2Ah must be set for the alias to work; if a zero is written to VRA, both sample rates are reset to 48k.

SR1[15:0] Writing to this register allows the user to program the sampling frequency from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hertz increments. Programming a value greater than 48 kHz or less than 7 kHz may cause unpredictable results.

Vendor ID Registers (Index 7Ch–7Eh)

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4144h

S[7:0] This register is ASCII encoded to “A.”

F[7:0] This register is ASCII encoded to “D.”

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5348h

T[7:0] This register is ASCII encoded to “S.”

REV[7:0] Revision Register field.

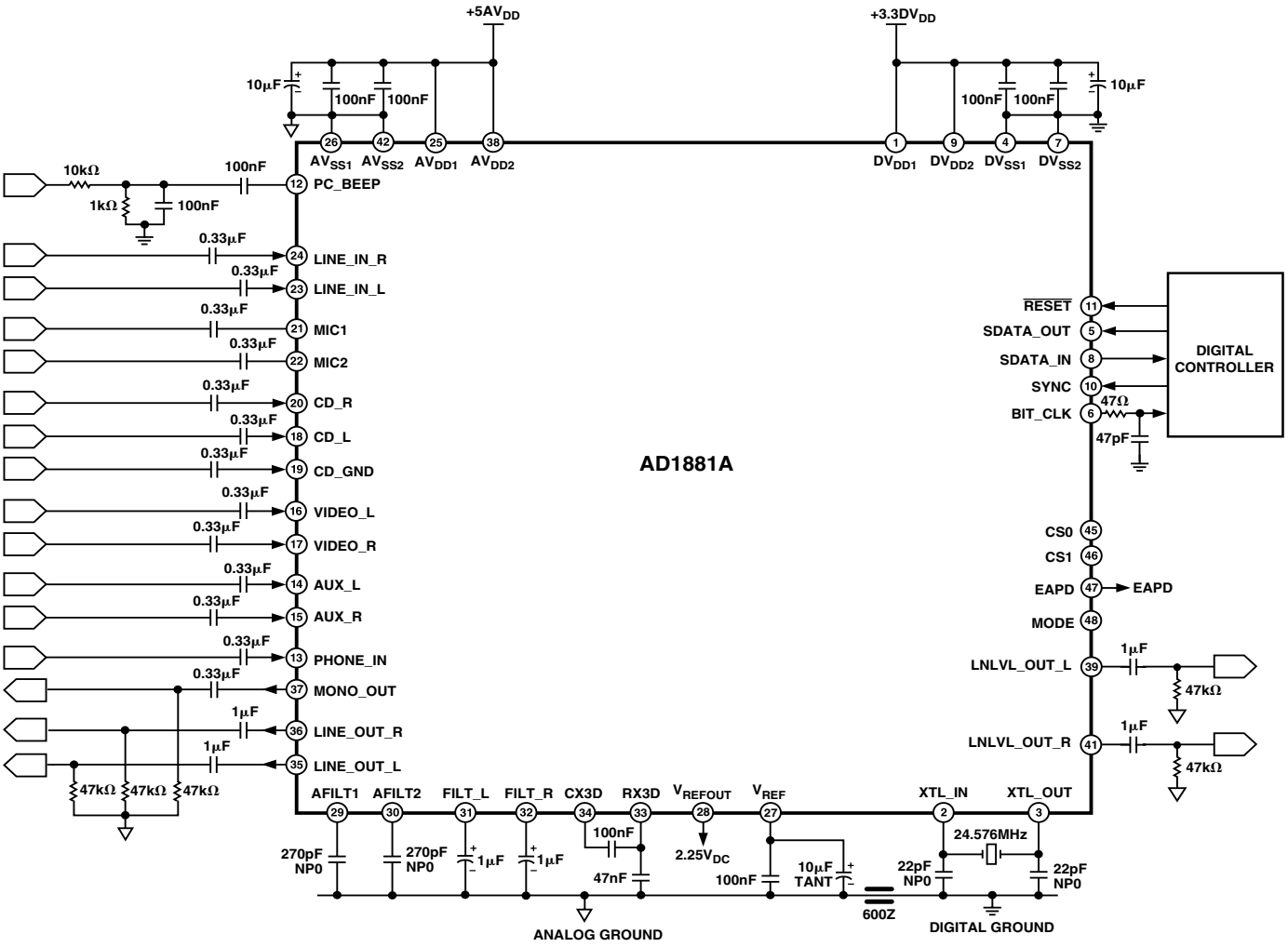
These bits are read-only and should be verified before accessing vendor defined features.

AD1881A/AD1881 USER VISIBLE DIFFERENCES

- Pin 48 is now MODE pin, no longer CHAIN_CLK.
- AD1881 chaining mode not supported.
- LSB of register 7Eh is 48h instead of 40h.

APPLICATIONS CIRCUITS

The AD1881A has been designed to require a minimum amount of external circuitry. The recommended applications circuits are shown in Figure 9. Reference designs for the AD1881A are available and may be obtained by contacting your local Analog Devices' sales representative or authorized distributor.



NOTE: FOR OPTIMAL PERFORMANCE USE A REGULATED ANALOG POWER SUPPLY.

Figure 9. Recommended One Codec Application Circuit

CD-ROM CONNECTIONS

The CD-ROM audio output level should be investigated; typical drives generate 2 V rms output and require a voltage divider for compatibility with the Codec input (1 V rms range). The recommended circuit is basically a group of divide-by-two voltage dividers as shown on Figure 10.

The CD_GND_REF pin is used to cancel differential ground noise from the CD-ROM. For optimum noise cancellation, this section of the divider should have approximately half the impedance of the right and left channel section dividers.

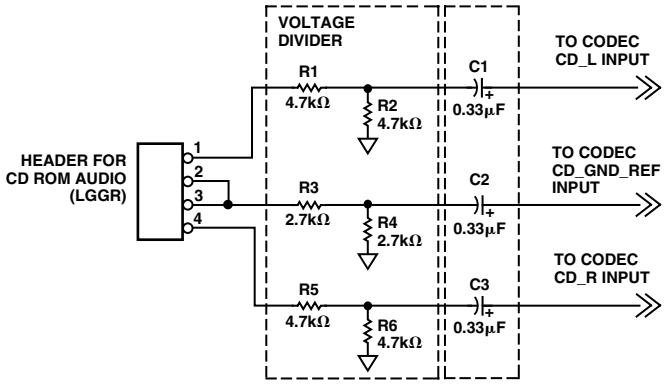


Figure 10. Typical CD-ROM Audio Connections

LINE_IN, AUX AND VIDEO INPUT CONNECTIONS

Most of these audio sources also generate 2 V rms audio level and require a –6 dB input voltage divider to be compatible with the Codec inputs. Figure 11 shows the recommended application circuit. For applications requiring EMC compliance, the EMC components should be configured and selected to provide adequate RF immunity and emissions control.

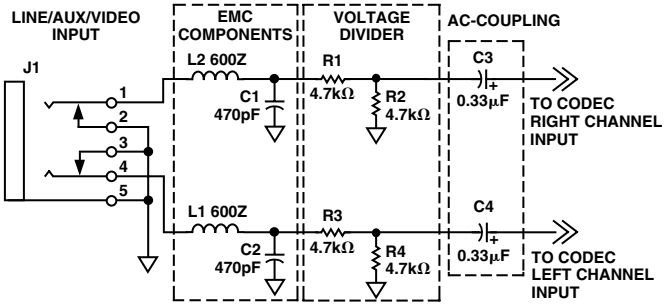


Figure 11. LINE_IN, AUX, and Video Input Connections

MICROPHONE CONNECTIONS

The AD1881A contains an internal microphone preamp with 20 dB gain, in most cases a direct microphone connection as shown in Figure 12 is adequate. If the microphone level is too low, an external preamp can be added as shown in Figure 13. In either case the microphone bias can be derived from the Codec's internal reference (V_{REFOUT}) using a 2.2 kΩ resistor. For the preamp circuit, the V_{REFOUT} signal can also provide the mid-point bias for the amplifier.

To meet the PC99 1.0A requirements, the MIC signal should be placed on the microphone jack tip and the bias on the ring. This configuration supports electret microphones with three conductor plugs, as well as dynamic microphones with two conductor plugs (ring and sleeve shorted together).

Additional filtering may be required to limit the microphone response to the audio band of interest.

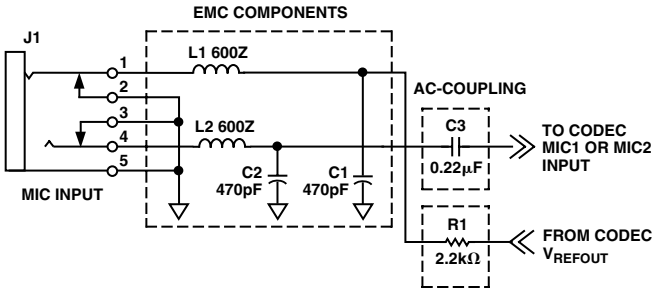


Figure 12. Recommended Microphone Input Connections

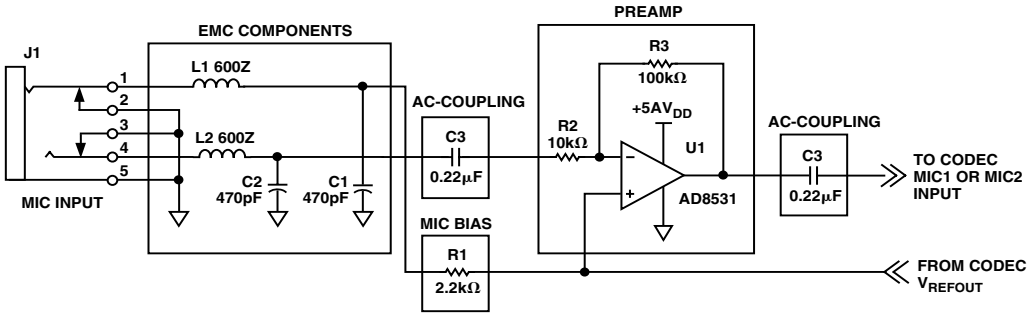


Figure 13. Microphone with Additional External Preamp (20 dB Gain)

LINE OUTPUT CONNECTIONS

The AD1881A Codec provides stereo LINE_OUT signals at a standard 1 V rms level. These signals must be ac-coupled before they can be connected to an external load. After the ac-coupling, a minimal resistive load is recommended to keep the capacitors properly biased and reduce click and pop when plugging stereo equipment into the output jack. The capacitor values should be selected to provide a desired frequency response, taking into account the nominal impedance of the external load. To meet the PC99 specification for PCs, testing must be performed with a 10 kΩ load, therefore a 1 μF value is recommended to achieve less than –3 dB roll-off at 20 Hz.

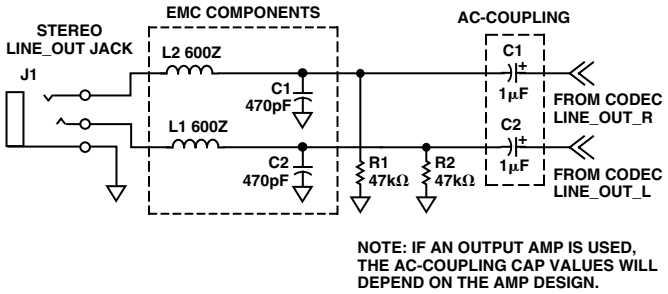


Figure 14. Recommended LINE_OUT Connections

USING AN EXTERNAL HEADPHONE/POWER AMP

The SSM2250 Power Amplifier is an ideal companion for the AD1881A. The amplifier can provide up to 250 mW output in stereo mode and up to 1.5 W into a mono speaker connected in a bridge-tied load (BTL) configuration.

The SM2250 has a mode control pin that can be used to switch between the stereo output mode and the mono BTL speaker.

Figure 15 shows a typical PC configuration where the SSM2250 drives a set of stereo headphones or external speakers, as well as an internal mono speaker. One of the normalizing pins on the stereo jack senses the stereo plug insertion and automatically switches from driving the internal mono speaker to driving the external stereo load.

To conserve power, the SSM2250 can be shut down by the EAPD pin on the AD1881A, using proper power management software. This is particularly important for portable applications. In shutdown mode, the SSM2250 consumes only 60 μA.

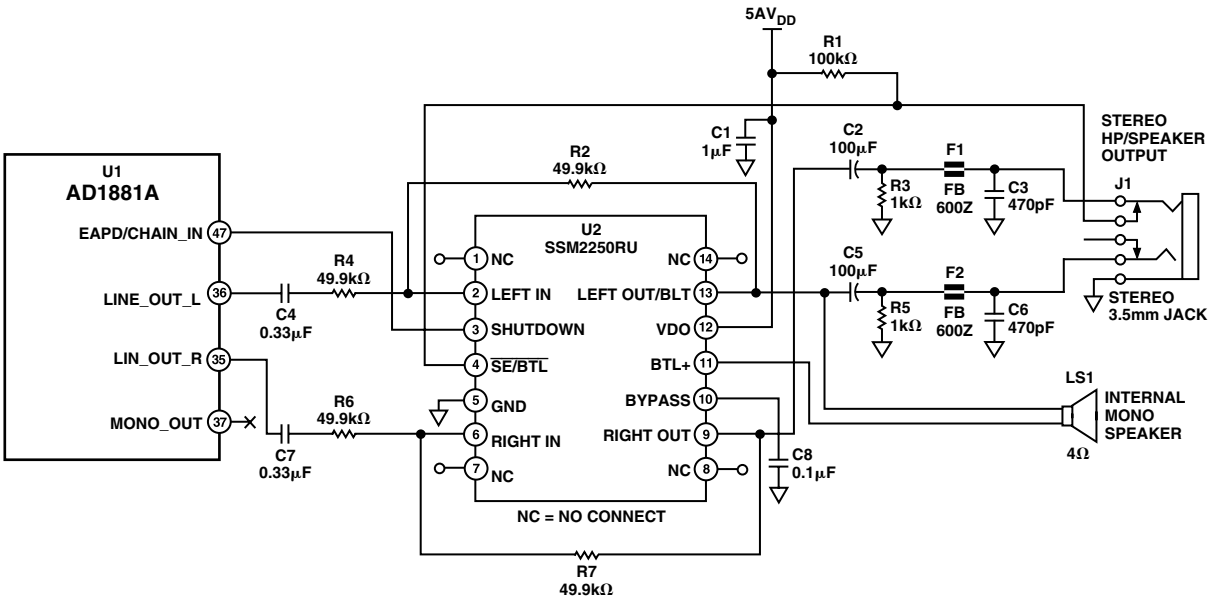


Figure 15. Using the SSM2250 Amplifier for Stereo and Mono Output

GROUNDING AND LAYOUT

To reduce noise and emissions, Analog Devices recommends a split ground plane as shown in Figure 16. The purpose of splitting the ground plane is to create a low noise analog area that is somewhat isolated from the digital ground current noise generated by the system's logic. All the analog circuitry should be placed on the analog ground plane area.

For reference purposes, and to return power supply currents, the analog and digital ground planes must be connected at some point, ideally a small bridge under or near the Codec should be provided. A 0 Ω resistor or a ferrite bead should also be considered since these allow some flexibility in optimizing the layout to meet EMC requirements.

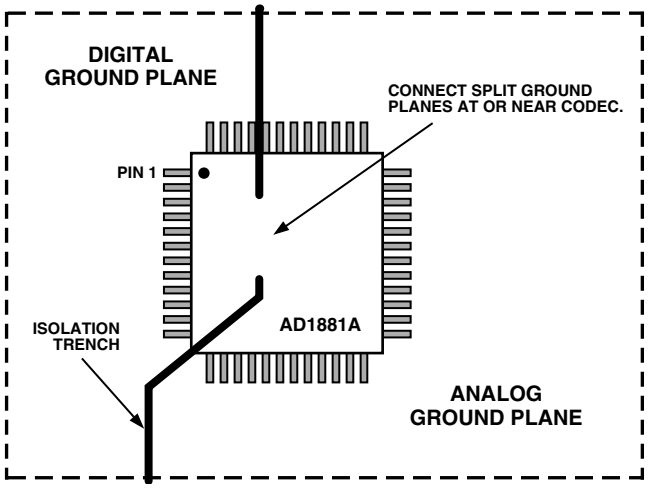


Figure 16. Recommended Split Ground Plane

ANALOG POWER SUPPLY

To minimize audio noise, the Codec analog power supply (AVDD) should be well decoupled and regulated. In PC systems it is recommended that the analog supply be derived from the 12 V PC power supply using a localized linear voltage regulator. Preferably, the analog power supply should be connected to the Codec's analog section using a ferrite bead.

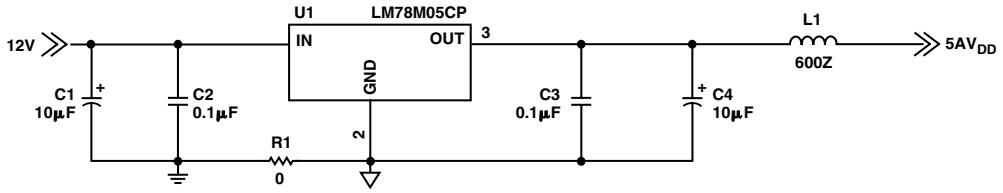


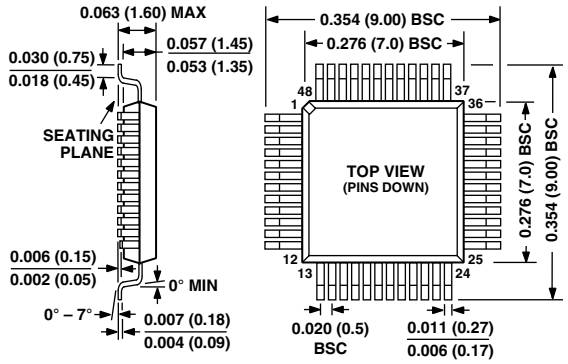
Figure 17. Recommended Regulator Circuit for Analog Power Supply

If a power plane layer is being used in the system design, it is recommended that the analog power plane for the Codec also be split (mirroring the analog ground plane). In this case, the analog power supply ferrite bead should bridge the isolation trench, close to the Codec location.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead Thin Plastic Quad Flatpack (LQFP)
(ST-48)



C3747–8–4/00 (rev. 0) 00752

PRINTED IN U.S.A.